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		(integrated adj circuit or asic) with (clock adj (skew or distribution) with (plural$3 adj blocks)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/20 10:01
L1	0	((semicondictor adj integrated adj circuit) or asic) same (clock adj skew) same (clock with data with parallel) and latch	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/20 08:24
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L3	0	((integrated adj circuit) or asic) with (clock adj skew) with (clock with data with parallel) and latch	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/20 08:25
L4	119	((integrated adj circuit) or asic) and (clock adj skew) and (clock with data with parallel) and latch	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/20 11:57
L5	25	((integrated adj circuit) or asic) same (clock adj skew) and (clock with data with parallel) and latch	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/20 08:26
L6	759	713/503	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/20 11:48
L7	5	4 and 6	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/20 08:50
L8	135	((integrated adj circuit) or asic) and (clock near2 skew) and (clock with data with parallel) and latch	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/20 08:52
L9	6	6 and 8	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/20 08:51

L10	3069	((integrated adj circuit) or asic) and (clock with data with parallel)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/20 08:53
L11	169	((integrated adj circuit) or asic) and (clock with data with parallel) and (single near4 substrate)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/20 08:53
L12	36	((integrated adj circuit) or asic) and (clock with data with parallel) and (single near4 substrate) and skew	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/20 09:07
L13	32	((semiconductor adj integrated adj circuit) or asic) and (clock with data with parallel) and (single near4 substrate) and skew	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/20 09:09
L14	10	((semiconductor adj integrated adj circuit) or asic) and (clock with data with parallel) and (single near4 substrate) and skew and (plurality near5 blocks)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/20 09:10
L15	5	("4639856" | "4689581" | "4827401" | "4890222" | "5095425").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2004/11/20 09:12
L19	1	(integrated adj circuit or asic) with (clock adj (skew or distribution)) with (plural$3 adj blocks)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/20 10:06
L20	8	(integrated adj circuit or asic) and (clock adj (skew or distribution)) with (plural$3 adj blocks)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/20 10:09
L21	47	(integrated adj circuit or asic) and (clock adj (skew or distribution)) and (plural$3 adj blocks)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/20 10:09
L23	3972	375/376	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/20 11:45

L24	2	23 and 4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/20 11:45
L25	1682	713/400	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/20 11:48
L26	12	25 and 4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/20 11:48
L27	91699	"712"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/20 11:57
L28	11	5 and 27	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/20 11:57
S1	1	"09/944134"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/10 06:39
S2	2	"6078623".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/19 10:42
S3	183741	takahashi.in.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/19 11:05
S4	346	takahashi-toshiro.in.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/19 11:05
S5	109	koide-kazuo.in.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/19 11:06

S6	24	S4 and S5	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/19 11:06
S7	4	"5-159080"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/19 11:07
S8	0	"11-202971"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/19 11:13
S9	0	"10-008932"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/19 11:13
S10	95	nakagawa-naoki.in.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/19 11:14
S11	11	egawa-kanji.in.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/19 11:14
S12	1	S10 and S11	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/19 11:14
S13	552	(integrated adj circuit or asic) with (clock adj skew)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/20 07:20
S14	2	(integrated adj circuit or asic) with (clock adj skew) with parallel	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/20 10:01
S15	3	(integrated adj circuit or asic) with (clock adj skew) with (phase adj adjustment)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/20 07:25

S16	0	(integrated adj circuit or asic) with (clock adj skew) with (clock with data with parallel)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/20 07:26
S17	2	(integrated adj circuit or asic) same (clock adj skew) same (clock with data with parallel)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/20 07:28
S18	1	(integrated adj circuit or asic) same (clock adj skew) same (clock with data with parallel) and latch	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/20 07:33
S19	0	(integrated adj circuit or asic) same (clock adj skew) same (clock with data with parallel) and latch and (plurality near circuit$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/20 07:33
S20	1	(integrated adj circuit or asic) same (clock adj skew) same (clock with data with parallel) and latch and circuit$1	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/20 08:23

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1. chet_tocci_electech_9|**Integrated-Circuit** Logic Families|Glossary
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2. Closing the Gap Between **ASIC** and Custom: An **ASIC** Perspective (PDF)
... the speed of an. **integrated circuit** is determined ... such as **clock skew** and. **latch** overheads, as about 30% sigda.org/Archives/.../Dac/Dac2000/papers/2000/dac00/pdffiles/39_1.pdf - 64k - View as html - More from this site

3. EP patents matching keyword 'clock'
... On chip **clock skew** control method and apparatus ... EP464632. **Parallel** data processing apparatus with sign gauss.bacon.su.se/indices/keyword/26 - 525k - Cached - More from this site

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EP patents matching keyword 'circuit' 7604 patents matches 'circuit' EP432723. Facsimile device enabling highly development and ... in an **integrated circuit** with a **parallel**-serial port ... signal distribution circuit with reduced **cl** gauss.bacon.su.se/indices/keyword/25 - 525k - Cached - More from this site

5. Northeastern Univeristy VLSI LAB.
Welcome to Northeastern University VLSI Laboratory! ... **Integrated Circuit** Design, Clocking scheme for high pe Reliable **Latch** Based Circuit ...
www.ece.neu.edu/faculty/ybk - 36k - Cached - More from this site

6. chet_tocci_electech_9|Introductory Concepts|Glossary
Introductory Concepts. Glossary. Access Time — Time between the memory's receiving a new input address and Number that uniquely identifies ... Application-Specific **Integrated Circuit** (**ASIC**) — An IC that ... — Signal used t wps.prenhall.com/chet_tocci_electech_9/0,8396,1039011-,00.html - 90k - Cached - More from this site

7. **ASIC**'95 Conference Information
1995 IEEE International **ASIC** Conference and Exhibit. It is with genuine pleasure that the Program Committee we incorporate application-specific **integrated circuit** (**ASIC**) technology. The ... A systolic **parallel** architecture is pr **asic**.union.edu/adv_prog_95.html - 102k - Cached - More from this site

8. Integrated Circuits for 2003
... a bank of 128 **parallel** matched filters of length 128 ... communication theory perspectives. An **ASIC** version of www.eecs.berkeley.edu/IPRO/Summary/03abstracts/chapter4.html - 109k - Cached - More from this site

9. type_Document_Title_here
... **integrated circuit** (**ASIC**) see **asic** ... **clock skew** 44, 45, 48, 68, 141, 170 elimination 90 clock central generat web.ukonline.co.uk/paul.naish/DA - 9k - Cached - More from this site

10. http://www.research.ibm.com/journal/rd/435/averill.txt
... is begun in **parallel** with the detailed logic ... Small refinements in **latch** boundaries can be ... in **parallel** for ea www.research.ibm.com/journal/rd/435/averill.txt - 105k - Cached - More from this site

11. Abstracts ICCAD '95
... of three-dimensional **integrated circuit** interconnect. However, to be ... of clock speeds, **clock skew** has beco ballade.cs.ucla.edu/~kohcc/.../iccad95/htmfiles/sun_sgi/iccadabs.htm - 265k - Cached - More from this site

12. Abstracts ICCAD '95
... of three-dimensional **integrated circuit** interconnect. However, to be ... of clock speeds, **clock skew** has beco
ballade.cs.ucla.edu/~kohcc/sigdacdrom/iccad95/papers/.../iccadabs.htm - 132k - Cached - More from this site

13. http://www.research.digital.com/wrl/DECarchives/DTJ/DTJH04/DTJH04SC.TXT
The AlphaServer 8000 Series: High-end Server Platform Development by David M. Fenwick, Denis J. Foley, Willi
application-specific **integrated circuit** (**ASIC**) components. The assemblies ... quoted system-wide **clock skew** o
www.research.digital.com/wrl/DECarchives/DTJ/DTJH04/DTJH04SC.TXT - 110k - Cached - More from this site

14. Veröffentlichungen
... static, dynamic, **latch**, data- precharged, and ... Annual IEEE Int'l **ASIC** Conf ... **clock skew** and system scale;
www-md.e-technik.uni-rostock.de/ma/gf94/institut/ergebnis.htm - 527k - Cached - More from this site

15. Digital Systems Design with VHDL and Synthesis - Preface
... array application-specific **integrated circuit** (**ASIC**) design process. ... Flip-flop, **latch**, and three-state buffer ...
www.computer.org/cspress/catalog/BP00023/preface.htm - 32k - Cached - More from this site

16. ACSEL-Advanced Computer Systems Engineering Laboratory
... **Parallel** and Distributed Computing, No. 5, pp. 716-728, 1988. V. G. Oklobdžija, "Architecture For Single-Chip
www.acsel-lab.com/Publications.html - 57k - Cached - More from this site

17. [Acken83]
References ... Wooley, "A two's complement **parallel** array multiplication algorithm," IEEE ... Tan, "Teaching cust
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18. Terms and Definitions
Computer Engineering (Processors) Terms and Definitions. Version: December 2, 1997. This is the proposed list
Specific **Integrated Circuit**. An **integrated circuit** ... bits are transmitted in **parallel**. Examples: a bit **parallel** ...
www-ece.engr.ucf.edu/~jza/glossary/terms.html - 279k - Cached - More from this site

19. Abstracts DAC'91
... caused by merging of **parallel** transistors is reduced ... correlation are close to **latch** outputs. Topology-based I
sigda.org/Archives/.../Dac/Dac91/papers/1991/dac91/dacabs.htm - 290k - Cached - More from this site

20. IBM Austin Research Lab | Achievements
... an automatic tool for **ASIC** timing closure, Cache Preconditioning for ... Clock generator for **integrated circuit**.
www.research.ibm.com/arl/achievements - 48k - Cached - More from this site

21. http://www-ee.eng.hawaii.edu/~msmith/Courses/Week/weekIX.htm
... activity-induced **clock skew** 17-20 ... PI, **parallel** in (boundary scan) 14-4 ... Simulation Program with **Integrate**
www-ee.eng.hawaii.edu/~msmith/Courses/Week/weekIX.htm - 246k - Cached - More from this site

22. FPGA FAQ comp.arch.fpga archives - messages from 500
... For instance, **clock skew** is of little concern ... reg add 2 to PC **latch** insn, read another 2 read ... design used
www.fpga-faq.com/archives/00500.html - 91k - Cached - More from this site

23. Michael Barr's Embedded Systems Glossary
A glossary of terms relevant to the development of software for embedded systems. ... address decoder. address
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www.netrino.com/Publications/Glossary - 118k - Cached - More from this site

24. Effect of increasing chip density on the evolution of computer architectures
IBM Journal of Research and Development issue 46-23, Scaling CMOS to the Limits - Effect of increasing chip de
dx.doi.org/10.1147/rd.462.0223 - 74k - Cached - More from this site

25. UNIVERSITY OF SURREY - MODULE CATALOGUE
UNIVERSITY OF SURREY - MODULE CATALOGUE. Module Short Name : L2U10 Module Title : DIGITAL ENGI

clocking arrangements; **clock-skew**. Alternative methods of ... The idea of an **ASIC**; full-custom and semi ...
www.open.mis.surrey.ac.uk/misweb/modules/4673.htm - 13k - Cached - More from this site

26. http://ilmukomputer.wankota.org/bukuputih/istilah-ti-indonesia.txt
... accumulator:akumulator: accumulator **latch**:grendel akumulator: accumulator ... lubang-abu: **ASIC**:**ASIC**: ASID
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(IC) designed for standalone ... separated into serial and **parallel** devices. These distinctions ... as a serial or **par**
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28. TO/TR
... based on the proportionality of the reactance of a **parallel** plate capacitor with large electrodes and their distan
www.steinbeis-europa.de/db/index.php4?topic=bbslist%26bbs_type=Offer - 525k - Cached - More from this site

29. EngPlanet Reference Link
A glossary of terms relevant to the development of software for embedded systems. ... address decoder. address
tick ...
www.engplanet.com/redirect.html?2679 - 121k - Cached - More from this site

30. http://www.funet.fi/pub/mirrors/wombat.doc.ic.ac.uk/foldoc/queries
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www.funet.fi/pub/mirrors/wombat.doc.ic.ac.uk/foldoc/queries - More from this site

31. słownik angielsko polski 2
... Pacific Daleki Wschód. **ASIC** (application-specific **integrated circuit**) specjalizowany układ scalony ... dwukier
elektronikjk.republika.pl/t4.html - 525k - Cached - More from this site

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1 **Clock skew reduction in ASIC logic design: a methodology for clock tree management**
Balboni, A.; Costi, C.; Pellencin, M.; Quadrini, A.; Sciuto, D.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Volume: 17 , Issue: 4 , April 1998
Pages:344 - 356

[Abstract] [PDF Full-Text (340 KB)] **IEEE JNL**

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2 **Delay-difference DLL and its-application on skewed output buffer**
Ya-Lan Tsao; Ming-Chao Chung; Shyh-Jye Jou;
ASIC, 2002. Proceedings. 2002 IEEE Asia-Pacific Conference on , 6-8 Aug. 2002
Pages:279 - 282

[Abstract] [PDF Full-Text (308 KB)] **IEEE CNF**

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3 **Self-tested self-synchronization by a two-phase input port**
Mu, F.; Svensson, C.;
ASIC Conference 1998. Proceedings. Eleventh Annual IEEE International , 13-16 Sept. 1998
Pages:259 - 262

[Abstract] [PDF Full-Text (388 KB)] **IEEE CNF**

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4 **Optimal buffered clock tree synthesis**
Jae Chung; Chung-Kuan Cheng;
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Pages:130 - 133

[Abstract] [PDF Full-Text (264 KB)] **IEEE CNF**

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5 **Demonstration of power enhancements on an industrial circuit through**

delay management of non-critical data paths
Velenis, D.; Tang, T.K.; Kourtev, I.S.; Adler, V.; Baez, F.; Friedman, E.G.;
ASIC/SOC Conference, 2001. Proceedings. 14th Annual IEEE International , 12-15 Sept. 2001
Pages:30 - 33

[Abstract] [PDF Full-Text (328 KB)] **IEEE CNF**

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6 **A quadratic programming approach to clock skew scheduling for reduced sensitivity to process parameter variations**
Kourtev, I.S.; Friedman, E.G.;
ASIC/SOC Conference, 1999. Proceedings. Twelfth Annual IEEE International , 15-18 Sept. 1999
Pages:210 - 215

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7 **Clock routing for high-performance ICs**
Jackson, M.A.B.; Srinivasan, A.; Kuh, E.S.;
Design Automation Conference, 1990. Proceedings. 27th ACM/IEEE , 24-28 June 1990
Pages:573 - 579

[Abstract] [PDF Full-Text (600 KB)] **IEEE CNF**

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1 **Synthesizing distributed buffer clock trees for high performance ASICs**
Neves, J.L.; Friedman, E.G.;
ASIC Conference and Exhibit, 1994. Proceedings., Seventh Annual IEEE International , 19-23 Sept. 1994
Pages:126 - 129

[Abstract] [PDF Full-Text (352 KB)] **IEEE CNF**

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2 **A reliable clock tree design methodology for ASIC designs**
Mely Chen Chi; Shih-Hsu Huang;
Quality Electronic Design, 2000. ISQED 2000. Proceedings. IEEE 2000 First International Symposium on , 20-22 March 2000
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[Abstract] [PDF Full-Text (216 KB)] **IEEE CNF**

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3 **Synchronous performance and reliability improvement in pipelined ASICs**
Soyata, T.; Friedman, E.G.;
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Pages:383 - 390

[Abstract] [PDF Full-Text (852 KB)] **IEEE CNF**

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4 **Clock skew reduction in ASIC logic design: a methodology for clock tree management**
Balboni, A.; Costi, C.; Pellencin, M.; Quadrini, A.; Sciuto, D.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Volume: 17 , Issue: 4 , April 1998
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5 **High-speed circuit design using skew-tolerant domino**
Zhang Liang; Chenqixin; Chengjunxia;
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Pages:844 - 847 Vol.2

[Abstract] [PDF Full-Text (253 KB)] IEEE CNF

6 **Clock driven design method (CDDM) for deep sub-micron ASICs**
Tanizawa, T.; Kawahara, S.;
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7 **0.5 µm 1 M gate CMOS SOG**
Ikeda, N.; Ishibashi, A.; Maeno, H.; Matsue, S.; Asahina, K.; Arakawa, T.; Kato, S.;
Custom Integrated Circuits Conference, 1993., Proceedings of the IEEE 1993 , 9-12 May 1993
Pages:23.2.1 - 23.2.4

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8 **A silicon compiler approach to the design of SOI ASIC's**
Bartholet, B.; White, M.; Priebe, G.W.; Kopman, M.; McGehee, D.; Griffin, M.;
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9 **A direct-skew-detect synchronous mirror delay for application-specific integrated circuits**
Saeki, T.; Minami, K.; Yoshida, H.; Suzuki, H.;
Solid-State Circuits, IEEE Journal of , Volume: 34 , Issue: 3 , March 1999
Pages:372 - 379

[Abstract] [PDF Full-Text (272 KB)] IEEE JNL

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Kai Zhu; Wong, D.F.;
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Pages:376 - 385

[Abstract] [PDF Full-Text (368 KB)] IEEE JNL

11 **Design self-synchronized clock distribution networks in an SoC ASIC using DLL with remote clock feedback**
Hyun Lee; Han Quang Nguyen; Potter, D.W.;
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Pages:248 - 252

[Abstract] [PDF Full-Text (320 KB)] IEEE CNF

12 **Pin allocation for clock routing**
Junwei Jiang;
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[Abstract] [PDF Full-Text (340 KB)] IEEE CNF

13 **Digital-phase aligner macro for clock tree compensation with 70 ps jitter**
Woeste, D.; Dina, M.; Nguyen, T.; Strom, J.;
Solid-State Circuits Conference, 1996. Digest of Technical Papers. 43rd ISSCC., 1996 IEEE International , 8-10 Feb. 1996
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